IN THE SPECIFICATION:

Please replace the paragraph on page 4, lines 19-22, with the following paragraph:

a1

Figures 4A and **4B** show a flowchart of the operation of the process for predicting bit line or driver failures in accordance with a preferred embodiment of the present invention.

Please replace the paragraph on page 8, line 22, to page 9, line 3, with the following paragraph:

a2

Turning now to **Figures 4A** and **4B**, a flowchart of the operation of the process for predicting bit line or driver failures is shown in accordance with a preferred embodiment of the present invention. Particularly, with respect to **Figure 4A**, the process begins with an event scan call for a processor. The process then reads the L2 cache status register (L2SR) (step **402**) and a determination is made as to whether a cache CE is detected (step **404**). If a cache CE is not detected, the process clears the error flag and all addresses in the error table and sets the error counter to zero (step **406**). Then, the process proceeds to step **418** in **Figure 4B** to end event scan processing.

Please replace the paragraph on page 9, lines 4-11, with the following paragraph:

a3

If a cache CE is detected in step **404**, a determination is made as to whether the CE flag is set (step **408**). If the CE flag is not set, the process sets the CE flag (step **410**), saves the L2 address and syndrome in the error table (step **412**), and sets the error position pointer to two (step **414**). Then, the process increments the error counter (step **416**) and proceeds to step **418** in **Figure 4B** to end event scan processing.

Please replace the paragraph on page 9, line 22, to page 10, line 1, with the following paragraph:

a4

If the error position pointer is not equal to five in step **424**, the process increments the error position pointer (step **428**). Returning to step **420**, if the new address equals the stored address, the process proceeds to step **428** to increment the error position pointer. Thereafter, a determination is made as to whether the error counter is less than five (step